REMARKS

The present Amendment is in response to the Office Action having a mailing date of May 30, 2003, the deadline to which has been extended by three (3) months from August 30, 2003 to November 30, 2003, by petition and payment of fees. Claims 1-29 are pending in the present Application. Applicant has amended claims 1, 11, 20, 23, and 24. Claims 17, 22, 25, and 29 have been canceled. Consequently, claims 1-16, 18-21, 23, 24, and 26-28 remain pending in the present Application.

Drawing Objections

The Examiner states:

> **The drawings are objected to because, in figure 6, the control inputs of the transistors of (602) are not labeled; figures 1, 2 and 4 should be labeled "prior art"; the recitation "a restore mechanism" in claims 16 and 21; "a state saving latch" in claims 17 and 23 are not shown in the drawings.**
>
> **A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.**

Applicant will appropriately label figures 1, 2, and 4 with the "prior art" label 10. Applicant submits that the restore mechanism is shown in figure 7 as element 716 and the recited savings latch is shown in Figure 8 as element 816. Finally, Figure 6 does not include control inputs. Therefore, Applicant submits that the elements are within the description of the application.

35 USC §112 Rejections

The Examiner states:

Claims 1-29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and/or clarification is required.

Regarding claim 1, the recitations "a first latch adapted to be coupled to a first power supply" and "a second latch coupled to the first latch and adapted to be coupled to a second power supply" are indefinite because it is unclear as to how the first and second latches are "adapted to be coupled to the first and second power supplies" According to the drawings the first and second latches are coupled directly to the first and second power supplies (V1, V2). The same analysis is true for the recitation "adapted to" in claims 11, 20, 23.

Applicant has removed all instances of "adapted to" from the claims.

The Examiner states:

Regarding claim 2, the recitation "in a power saving mode, the voltage of at least one of the first and second power supplies is reduced" is indefinite because it is unclear how the voltage of the first or the second power supply can be reduced. Figures 6-8 show that the power supplies (V1) and (V2) are directly connected to the latches. There are no devices or circuits that are utilized to vary the power voltages as recited.

Applicant respectfully disagrees.

Applicant submits that it is well known to vary the voltage via a voltage regulator, voltage divider, or a voltage down converter. There are many ways to implement this, and one of ordinary skill in the art readily recognizes that these power supplies can be used.

The Examiner states:

Regarding claim 3, the recitation "in a power saving mode, the voltage of the power supply coupled to the latch which contains contents to be preserved is reduced to a voltage to preserve the state of the contents and the other power supply is reduced to substantially zero volts" is indefinite for the same reason raised in the rejection of claim 2.

The arguments with respect to claim 2 apply with the same force to this claim 3.

The Examiner states:

Regarding claims 17 and 23, the recitation "a state saving latch" is indefinite because it is misdescriptive. Figures 6-8 of the present application show only two latches: the master latch (602) and the slave latch (604). The Applicant is requested to show the "a state saving latch" in the drawings. It is also unclear as to the "state saving latch" on line 18 is the same or different than the "slave latch" on line 16.

As before mentioned the state saving latch is element 816, in figure 8.

The Examiner states:

Regarding claim 22, the recitation "a state saving latch" is indefinite because it is not clear as to this "a state saving latch" is the same or different than the "slave latch in claim 20.

The argument made with respect to claim 17 and 23 apply with equal force. Regarding claim 24, the recitation "providing a first independently controllable power supply coupled to the first latch; (b) providing a second independently controllable power supply coupled to the second latch; and c) reducing the voltage of at least one of the first and second power supplies responsive to the detection of a power saving mode" is indefinite because it is misdescriptive. Figures 6-8 of the present application shows that there are no devices used to vary the supply voltages (V1) and (V2). The same analysis is true for the recitation "controllable power supply" in claim 29.

Applicant submits that a controllable power supply is well known and reducing the voltage of these power supplies, are well known. Therefore, applicant submits that this recitation is clear and definite.

The Examiner states:

Regarding claim 29, the recitation "detecting the normal mode" is indefinite because it is unclear how a normal mode can be detected. There is no detection circuit shown in the drawings.

Claim 29 has been canceled.

Applicant submits that with the above amendments and arguments, the claims are now clear and definite and the rejection of the claims under 35 USC 112 has been overcome.

35 USC §102 Rejections

The Examiner states:

Claims 1-7, 18, 19 and 24-29, insofar as understood, are rejected under 35 U.S.C. 102(e) as being anticipated by Ooishi (US Pat. 6,433,586).

Regarding claims 1 and 2, figures 4, 6A, 6B and 7 show a flip-flop comprising: a first latch (22) "adapted" to be coupled to a first power supply (PSO); and a second latch (24) coupled to the first latch and adapted to be coupled to a second power supply (PS1), wherein the first and second power supplies are independently controllable to minimize power consumption when the flip-flop is in a power saving mode. Note that in the sleep mode (saving mode) the voltage of the first power supply (PS0) becomes 0 volt and the voltage of the second power supply (PS1) is coupled to the voltage (VBST), Node (NS1) is coupled to (VCC/2) for reducing the leakage current thus, the power consumption is minimized (col. 11, lines 37-49, col. 14 lines 14-19).

Regarding claim 3, figures 6A, 6B, and 7 show that during the sleep mode, the supply voltage (PSO) of the master latch reduces to 0 volt and the control voltage (NS1) of the slave latch that preserves the data is raised to an intermediate voltage (VCC/2) thus, the power consumption of the master-slave flip-flop is reduced (col. 11, lines 37-50, col. 14, lines 13-20).

Regarding claims 4, 5, 6 and 7, the first latch (22) is a master latch and the second latch (24) is a slave latch. The first clock is (TG1) and the second clock is (TG2). (TG1) and (TG2) are free running clocks.

Regarding claims 18 and 19, in the sleep mode, (PSO) is reduced to 0 volt and the voltage across the slave latch (24) that preserves the "contents" is reduced by bringing up the voltage at (NS1) to (VCC/2) (col. 11, lines 43-49, col. 14, lines 13-20).

Regarding claims 24 and 25, figures 4, 6A, 6B and 7 show a method for minimizing the power consumption of a flip-flop, the flip-flop including a first latch (22) and a second latch (24) coupled thereto; the method comprising the steps of:

(a) providing a first independently controllable power supply (PSO) coupled to the first latch;

(b) providing a second independently controllable power supply coupled to the second latch (PS1); and

(c) reducing the voltage of at least one of the first (PS1 is reduced to volt) and second power supplies (PS1) responsive to the detection of a power saving mode. Note that in the power saving mode (sleep mode), (PS1) is reduced to 0 volt (col. 11, lines 37-49) and the voltage across the slave latch (24) is reduced by bringing up the voltage at (NS1) to VCC/2 (col. 14, lines 13-20). Thus, the power consumption of the flip-flop is reduced. Note that the slave latch (24) supplied by (PS1) that "preserves" the "contents" has the supply (PS1) is reduced by raising the voltage of (NS1) and supply (PS0) is reduced to 0 volt.

Regarding claims 26, 27 and 28, the first latch (22) is a master latch and the second latch (24) is a slave latch. The first clock is (TG1) and the second clock is (TG2).

Regarding claim 29, figures 4, 6A, 6B and 7 show a method for returning normal mode from power saving mode to preserve the contents in a flip-flop, the flip-flop including a first latch and a second latch coupled thereto, the method comprising the steps of:

(a) providing a first independently controlling power supply (PS1) coupled to the second latch (24) wherein the at least one of the first and second power supplies is at substantially zero volts and the other of the first and second power supplies is at a reduced voltage such that the state of the contents in the associated latch is preserved;

(c) When the normal mode is desired the first and second power supplies is restore to full values (VCC) (col. 10, lines 47-55).

35 USC §103 Rejections

The Examiner states:

Claims rejected under 35 U.S.C. 103(a) as being unpatentable over Ooish (US Pat. 6,433,586).

Regarding claims 8-10, figure 4 of Ooishi includes all the limitation of claims 8-10 except for the limitations that the first clock is gated and the second clock is free running; the first clock is free running and the second clock is gated. The first clock is gated and the second clock is gated. However, it is old and well known in the art that a gated clock coupled to a device is used to control that device by turning it on or by turning it off. By turning off the clock, the device is disabled. Therefore, it would have been obvious to those skilled in the art to implement the gate to the clocks of the flip-flops of Ooishi to control the functional modes of the flip-flop. For instance, if the two gated clock are

disabled, the flip-flop will stop working. The master-slave flip-flop works as a single latch if only one of the gated clock is enabled.

Claims 11, 12-17 and 20-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ooishi (US Pat. 6,433,586) in view of Barbier et al. (US Pat. 5,777,489).

Regarding claims 11, 12, 20 and 23, figures 4, 6A, 6B and 7 of Ooishi include all the limitations of the present application except for the limitation that there is a multiplexor coupled to the first and second latch. Figure 2 of Barbier shows a master-slave flip-flop having a multiplexor (208) coupled to the outputs of the master latch (204) and to the output of the slave latch (206) for selecting the output of the master latch or the slave latch for performing a desired function (col. 3, lines 48-67). Therefore, it would have been obvious to those skilled in the art to implement the multiplexor taught by Barbier to the master-slave circuit of Oosihi for the selection of the latch outputs. (208) is a shunt multiplexor. Note that in the sleep mode, the power supply (PSO) is reduced to 0 volt and the power supply (PS1) is reduced to a lower value by bringing the voltage at node (NS1) to (VCC/2) (See Ooishi col. 11 and 14).

Regarding claims 13, 14, 15 and 16, figure 5 of Ooishi shows that during a first clock (TG1) one bit of data (D2) is latched by the first latch (22). The first latch (22) is a master latch and the second latch (24) is a slave latch. The "a restore mechanism" is the multiplexor (208).

Regarding claim 17, the "state saving latch" is element (24) that is activated only in the standby power mode (sleep mode). Note that in the sleep mode latch (22) is turned off and latch (24) is turned on with a low supply voltage (PS1).

Regarding claim 21, the "restore mechanism" is the multiplexor (208).

Regarding claim 22, the "state saving latch" is latch (24)

Applicant respectfully traverses these rejections.

PRESENT INVENTION

A flip-flop is disclosed in which power consumption is reduced in a standby mode. In a first aspect, the flip-flop comprises a first latch adapted to be coupled to a first power supply and a second latch coupled to the first latch and adapted to be coupled to a second power supply. The first and second power supplies are independently controllable to minimize power consumption in a standby mode.

ARGUMENTS

Independent claim 1, 11, 20, and 24 are reproduced in their entirety herein.

1. A flip-flop comprising:
a first latch coupled to a first power supply; and
a second latch coupled to the first latch and coupled to a second power supply, wherein the first and second power supplies are independently controllable to minimize power consumption when the flip-flop is in a power saving mode, and
a state saving latch which is coupled to the second power supply and is only activated upon detection of standby power saving mode; wherein the contents of the first latch are loaded into the state saving latch, wherein the first power supply is reduced to 0 volts and the second power supply is reduced to minimum voltage to sustain the state.

11. A flip-flop comprising:
a first latch coupled to a first power supply, the first latch for receiving at least one bit;
a second latch coupled to the first latch and coupled to a second power supply, the second latch for storing the at least one bit from the first latch, wherein the size of the second latch is minimized to reduce power consumption; and
a multiplexor coupled to the first latch and to the second latch for outputting the at least one bit from the first latch when a clock to the multiplexor is active and for outputting the at least one bit from the second latch when the clock is inactive, wherein the first and second power supplies are independently controllable; and
a state saving latch which is coupled to the second power supply and is only activated upon detection of standby power saving mode; wherein the contents of the first latch are loaded into the state saving latch, wherein the first power supply is reduced to 0 volts and the second power supply is reduced to minimum voltage to sustain the state.

20. A flip-flop comprising:

a master latch coupled to a first power supply, the master latch for receiving at least one bit; and

a slave latch coupled to the master latch and coupled to a second power supply, the slave latch for storing the at least one bit from the master latch wherein the size of the latch is minimized to reduce power consumption; and

a shunt multiplexor coupled to the master latch and to the slave latch for outputting the at least one bit from the master latch when a clock to the multiplexor is active and for outputting the at least one bit from the slave latch when the clock is inactive; and

a state saving latch which is coupled to the second power and is only activated upon detection of standby power saving mode; the voltage of the power supply coupled to the state saving latch which contains contents to be preserved is reduced to a voltage to preserve the state of the contents and the other power supply is reduced to substantially zero volts.

23. A flip-flop comprising:

a master latch coupled to a first power supply, the master latch for receiving at least one bit; and

a slave latch coupled to the master latch and coupled to a second power supply, the slave latch for storing the at least one bit from the master latch wherein the size of the latch is minimized to reduce power consumption.

a shunt multiplexor coupled to the master latch and to the slave latch for outputting the at least one bit from the master latch when a clock to the multiplexor is active and for outputting the at least one bit from the slave latch when the clock is inactive, the voltage of the power supply coupled to the latch which contains contents to be preserved is reduced to a voltage to preserve the state of the contents and the other power supply is reduced to substantially zero volts;

a restore mechanism which multiplexes the data and an output of the slave latch to enable recovery of the state of the contents of the master latch; and

a state saving latch which is coupled to the second power supply and is only activated upon detection of the power saving mode, the voltage of the power supply coupled to the state saving latch which contains contents to be preserved is reduced to a voltage to preserve the state of the contents and the other power supply is reduced to substantially zero volts.

24. A method for minimizing the power consumption of a flip-flop, the flip-flop including a first latch and a second latch coupled thereto; the method comprising the steps of:

(a) providing a first independently controllable power supply coupled to the first latch;

(b) providing a second independently controllable power supply coupled to the second latch; and

(c) reducing a voltage of at least one of the first and second power supplies responsive to the detection of a power saving mode wherein, in a power saving mode, the voltage of the power supply coupled to a state saving latch which contains contents to be

preserved is reduced to a voltage to preserve the state of the contents and the other power supply is reduced to substantially zero volts.

All the independent claims have been amended to include the state saving latch. The contents to be preserved are loaded into the state saving latch from the master latch when the circuit is in the power saving mode. This state saving latch is neither taught or suggested by the cited references. Accordingly, applicant submits that the independent claims are allowable over the cited references. Since the independent claims are allowable the claims dependent thereon are allowable. Applicant respectfully requests therefore, reconsideration and allowance of the claims as now presented.

Applicant's attorney believes that this application is in condition for allowance. Should any unresolved issues remain, Examiner is invited to call Applicant's attorney at the telephone number indicated below.

Respectfully submitted,

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November 26, 2003
Date

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